REMARKS

Claims 1-30 are pending. Claims 1-30 were rejected. Independent claims 1, 19, 24, and 30 were rejected under 35 U.S.C. 102(e) as being anticipated by (U.S. Patent No. 6,080,201) Hojat.

The Examiner identified particular portions of the specification and particular language in the claim interpretation section of the Office Action. It should be noted, however, that the claims not be fully interpreted without considering plain meaning, the specification in its entirety, and/or other intrinsic evidence.

The independent claims of the present invention were rejected using Hojat. Hojat describes a "method for improving timing convergence in computer aided semiconductor circuit design" (Abstract). Hojat describes extracting "information from the placement state provided to determine the lengths of individual nets after placement" (8:54-57). "Of course, after the first few cuts, the partitions will be large and each partition will contain multiple placeable objects. When there is more than one placeable object in a partition, each object is presumed to be in the center of the partition. In this case, the synthesizer utilizes conventional statistical models to determine the net lengths for nets connecting objects in the same partition. For objects in different partitions, the synthesizer uses conventional maze routing schemes to determine the netlengths" (8:61-9:2).

However, Hojat does not teach or suggest determining a statistical estimate for a "future" delay corresponding to a "future" connection placed across a boundary. By contrast, the independent claims 1, 24, and 30 all variably recite "determining a statistical estimate for a future delay" associated with a "future connection" to be placed across a "second boundary." Independent claim 19 recites generating "statistical estimates" for "future delays" on "uncut connections." According to various embodiments, the techniques of the present invention allow more accurate estimation of "delays for connections which have not yet been placed" (page 6, lines 4-5).

The Examiner argued that Hojat "teaches the cutting of the design and the subsequent timing analysis where statistical analysis is used to determine the net lengths for nets connecting objects in the same partition. When the process is repeated (elements 204-216), the design is

again "cut" and the objects connected in the same partition will now be separated into different partitions." Therefore, the Examiner argues "that the objects that were connected in the same partition are now connected across a boundary and thus the statistical estimate used for the connection of objects inside the same partition is an estimate for a "future" delay corresponding to the "future" connection placed across a boundary that will occur when the circuit is cut again."

The Applicants respectfully disagree. Hojat explicitly mentions that is uses "conventional maze routing schemes to determine netlengths" (9:1-3). "After each cut... "timing checks of the paths in the circuit" are made. (8:45-53). Timing checks are performed only for placeable objects that are presumed to be in the same partition or "in the center of the partition." (8:61-9:2) No timing estimates are made for any connections that are placed across partitions. No consideration for future cuts is made.

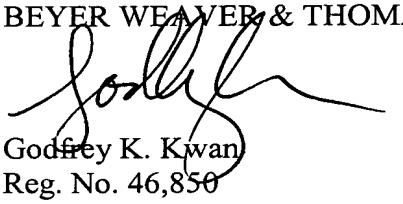
According to various embodiments, the techniques of the present invention allow more accurate estimation of "delays for connections which have not yet been placed" (page 6, lines 4-5). That is 'after this partition phase, criticality of a path is determined by a combination of delays associated with the actual cuts (such as the cut on connection 203) and an estimate as to future cuts. In conventional partitioning, the estimate is based only on the number of uncut connections." (Page 14, lines 14-18) Hojat describes only making estimates for objects presumed to be uncut.

Hojat only describes "statistical models to determine the net lengths for nets connecting objects in the same partition" and "maze routing schemes to determine the netlengths" for nets connecting objects in "different partitions" (8:61-9:2). There is no mention or suggestion of estimating "future" delays for "future" or "uncut" connections.

Although the claims are believed patentable in their current form, amendments are being made to further clarify the claims and facilitate prosecution. Independent claim 1 is being amended to recite "wherein the statistical estimate for the future delay is made using estimates of future cuts." Nothing in Hojat suggests using estimates of future cuts. Independent claim 19 is being amended to recite "generating statistical data corresponding to each type of boundary crossed in the target device, wherein the statistical data is generated using estimates of future cuts." Hojat does not teach or suggest generating statistical data using estimates of future cuts.

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicants believe that all pending claims are allowable in their present form. Please feel free to contact the undersigned at the number provided below if there are any questions, concerns, or remaining issues.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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